WHAT IS CLAIMED IS:

1. A circuit for turning on an internal voltage rail comprising:

a first transistor coupled between a power supply node and an internal voltage rail node;

a second transistor coupled to a control node of the first transistor;

a third transistor coupled to the second transistor and having a control node coupled to the control node of the first transistor;

a fourth transistor coupled between the second transistor and the power supply node; and

a fifth transistor coupled between the third transistor and the power supply node, wherein the third transistor is coupled between the second transistor and the fifth transistor.

2. The circuit of claim 1 wherein the first, second, third, fourth, and fifth transistors are MOS transistors.

3. The circuit of claim 1 wherein the first, third, fourth, and fifth transistors are a first conductivity type, and the second transistor is a second conductivity type.

4. The circuit of claim 1 wherein the first, third, fourth, and fifth transistors are PMOS transistors, and the second transistor is an NMOS transistor.

5. The circuit of claim 1 further comprising:

a first inverter coupled to a control node of the fourth transistor;

a second inverter coupled to a control node of the fifth transistor; and

a buffer coupled to a control node of the second transistor.

6. The circuit of claim 1 further comprising internal circuitry coupled to the internal voltage rail node.

7. The circuit of claim 1 further comprising:

a first input node coupled to a control node of the second transistor;

a second input node coupled to a control node of the fourth transistor; and

a third input node coupled to a control node of the fifth transistor.

8. A method for turning on an internal voltage rail comprising:

coupling a first transistor between a power supply node and an internal voltage rail node;

mirroring a current from a second transistor to the first transistor during a turn-on time period; and

coupling a control node of the first transistor to a bias voltage node after the turn-on time period.

9. The method of claim 8 wherein the bias voltage node is a ground node.

10. The method of claim 8 further comprising coupling a third transistor between the second transistor and the bias voltage node for coupling the control node of the first transistor to the bias voltage node.

11. The method of claim 10 further comprising coupling a fourth transistor between the second transistor and the power supply node, wherein the fourth transistor is turned on during the turn-on time period and turned off after the turn-on time period.

12. The method of claim 11 further comprising coupling a fifth transistor between the third transistor and the power supply node, wherein the fifth transistor is turned off to allow the first transistor to turn on.